ABSTRACT OF DISCLOSURE

A three-dimensional (3-D) integrated chip system is provided with a first wafer including one or more integrated circuit (IC) devices; a second wafer including one or more integrated circuit (IC) devices; and metallic lines deposited on opposing surfaces of the first and second wafers at designated locations with an interlevel dielectric (ILD) recess surrounding the metallic lines to facilitate direct metal bonding between the first and second wafers and establish electrical connections between active IC devices on the first and second wafers.